17. A device comprising:

a p-well region;

a first High-Voltage N-type Well (HVNW) region and a second HVNW region contacting opposite edges of the p-well region;

a P-type Buried Layer (PBL) having opposite edges in contact with the first HVNW region and the second HVNW region;

a n-type buried well region underlying the PBL, wherein the p-well region and the n-type buried well region are in contact with a top surface and a bottom surface, respectively, of the PBL;

a first n-well region in a top portion of the p-well region;

a first n-type source region in the first n-well region;

a first gate stack overlapping a portion of the p-well region and a portion of the second HVNW region; and

a first channel region under the first gate stack, wherein the first channel region interconnects the first n-well region and the second HVNW region.

18. The device of claim **17**, wherein the first HVNW region and the second HVNW region are interconnected through an electrical path, with an entirety of the electrical path consisting of n-type regions.

19. The device of claim **18**, wherein the n-type buried well region is in physical contact with the first HVNW region and the second HVNW region.

20. The device of claim **17** further comprising:

a second n-well region in a top portion of the p-well region, wherein the first n-well region and the second n-well region are separated from each other by a portion of the p-well region;

a second n-type source region in the second n-well region;

a second gate stack overlapping a portion of the p-well region and a portion of the first HVNW region; and

a second channel region under the second gate stack, wherein the second channel region interconnects the second n-well region and the first HVNW region.

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